FEATURES

- Proprietary multiplier design for minimum THD
- Very accurate adjustable output over voltage Protection
- Ultra-low (30μA) Start-up current
- Low (2.5mA) quiescent current
- Digital leading-edge blanking on current sense
- Disable function on E/A input
- 1.4% (@ TJ = 25 °C) internal reference voltage
- -600/+800mA totem pole gate driver with active pull-down during UVLO and voltage clamp
- DIP-8/SO-8 packages

DESCRIPTION

The SMD630 is a current-mode PFC controller operating in Transition Mode (TM). The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

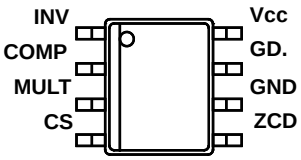
The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1.4% @TJ = 25°C) internal voltage reference.

The device features extremely low consumption (60μA max. before start-up and <5 mA operating) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving requirements

APPLICATIONS

- AC/DC LED Driver applications
- RGB Backlighting LED Driver
- Back Lighting of Flat Panel Displays
- Desk Top PC/ NB & Server application
- Game/ Printer application
- Chargers

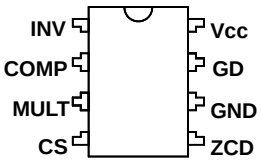
PACKAGE/ORDER INFORMATION



8-Pin Plastic S.O.I.C.
(Top View)

Order Part Number

SMD630PT



8-Pin Plastic DIP
(Top View)

SMD630J

PIN FUNCTIONS

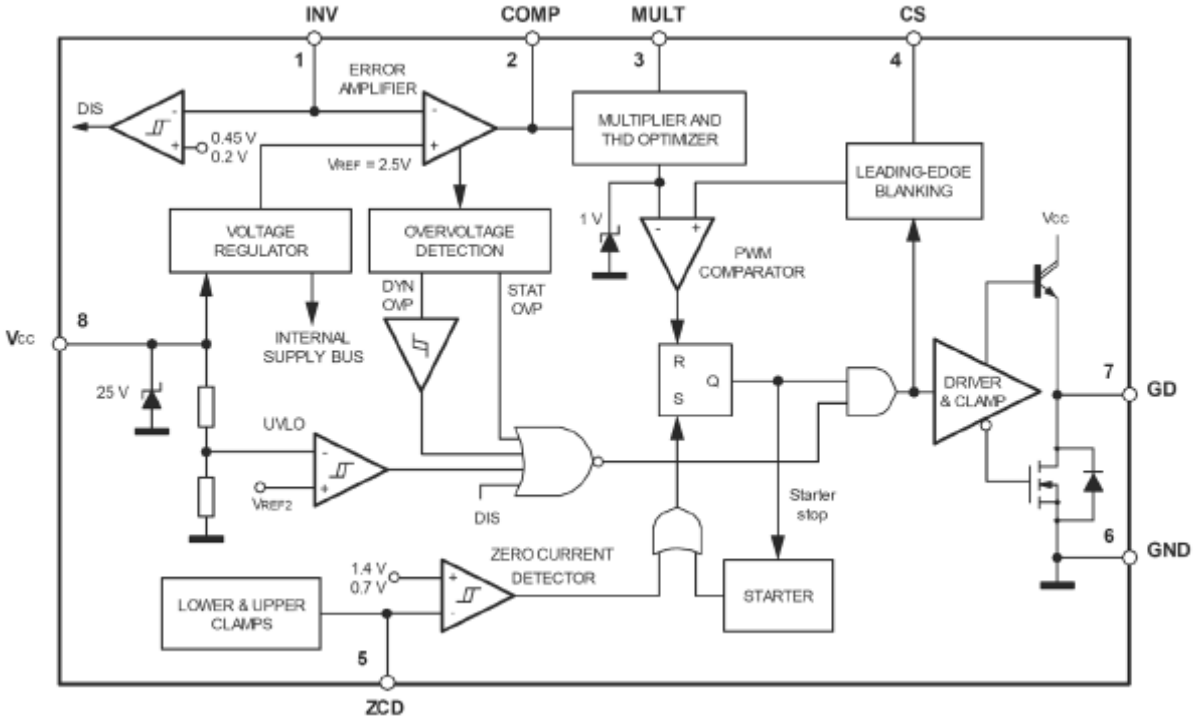
Pin No.	Pin Name	Function
1	INV	Inverting input. This pin doubles as an ON/OFF control input.
2	COMP	A compensation network is placed between this pin and INV
3	MULT	Main input to multiplier
4	CS	The current sensor input to determine MOSFET source pin
5	ZCD	Zero cross determine
6	GND	Ground
7	GD	Gate driver output
8	VCC	Supply voltage

ABSOLUTE MAXIMUM RATINGS (Note 1)

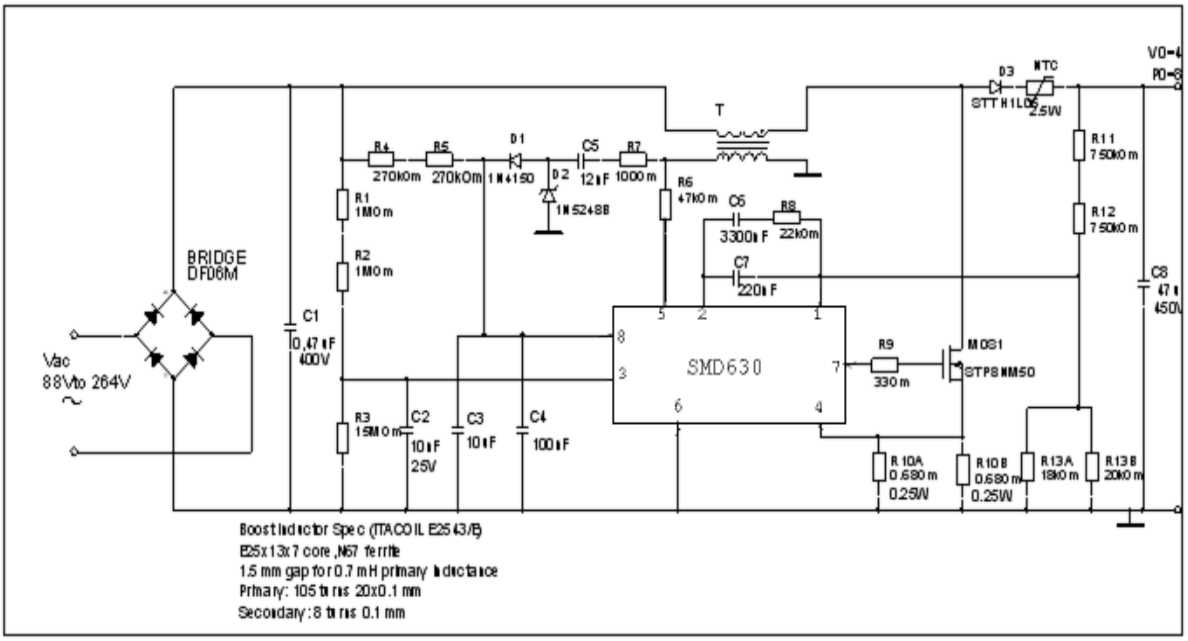
V_{CC} to GND	Self-limited
CS, MULT, COMP, INV	-0.3V to 8V
GATE to GND	Self-limited
Continuous Power Dissipation (TA = 50°C) (Note 1)	
8 Pin DIP (derate 9mW/°C above +50°C	1000mW
8 Pin SO (derate 6.3mW/°C above +50°C	650mW
Junction Temperature	-40°C to +150°C
Storage Temperature Range	-55°C to +150°C

Note 1: Exceeding these ratings could cause permanent damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

BLOCK DIAGRAM



TYPICAL APPLICATIONS



ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 25 °C.

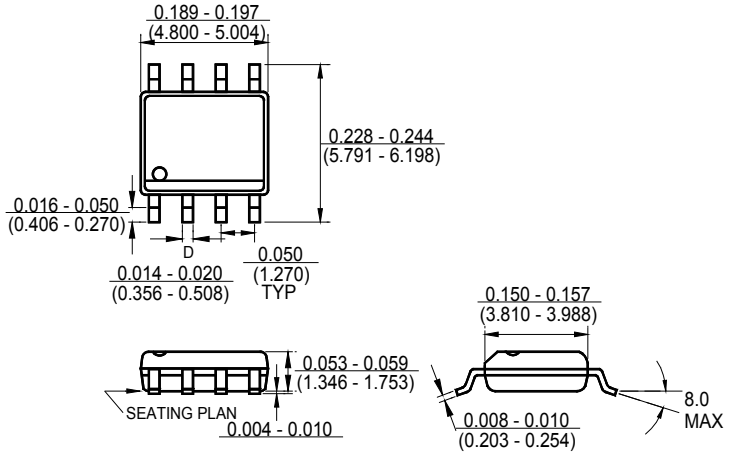
Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Supply voltage						
Operating range	After turn-on	V_{CC}	10.5		22.5	V
Turn-on threshold		V_{CCOn}	11.7	12.5	13.3	V
Turn-off threshold		V_{CCOFF}	9.5	10	10.5	V
Hysteresis		Hys	2.2		2.8	V
Zener Voltage	I_{cc} = 20mA	V_Z	23	25	27	V
Supply current						
Start-up current	Before turn-on, VCC = 11V	$I_{start-up}$		30	60	µA
Quiescent current	After turn-on	I_q		2.5	3.75	mA
Operating supply current	@ 70kHz	I_{cc}		3.5	5	mA
Quiescent current	During OVP (either static or dynamic) or VINV ≤150mV	I_q		1.7	2.2	mA
Multiplier input						
Input bias current	V_{MULT} = 0 to 4V	IMULT			-1	µA
Linear operation range		VMULT	0 to 3			V
Output max. slope	V_{MULT} = 0 to 1V, V_{COMP} = Upper clamp	$\frac{\Delta V\ cs}{\Delta V_{MULT}}$	1	1.1		V/V
Gain (2)	V_{MULT} = 1V, VCOMP= 4V,	K	0.32	0.38	0.44	V
Error amplifier						
Voltage feedback input threshold	TJ = 25 °C	V_{INV}	2.475	2.5	2.525	V
	10.5V < VCC < 22.5V (1)		2.455		2.545	
Line regulation	V_{CC} = 10.5V to 22.5V			2	5	mV
Input bias current	V_{INV} = 0 to 3V	I_{INV}			-1	µA
Voltage gain	Open loop	Gv	60	80		dB
Gain-bandwidth product		GB		1		MHz
Source current	V_{COMP} = 4V, V_{INV} = 2.4V	I_{COMP}	-2	-3.5	-5	mA
Sink current	V_{COMP} = 4V, V_{INV} = 2.6V		2.5	4.5		

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Upper clamp voltage	ISOURCE = 0.5mA	V_{COMP}	5.3	5.7	6	V
Lower clamp voltage	ISINK = 0.5mA (1)		2.1	2.25	2.4	V
Disable threshold		V_{INVdis}	150	200	250	mV
Restart threshold		V_{INVen}	380	450	520	mV
Output overvoltage						
Static OVP threshold			2.00	2.15	2.30	V
Current sense comparator						
Input bias current	V_{CS} = 0	I_{CS}			-1	µA
Leading edge blanking		t_{LEB}	100	200	300	ns
Delay to output		$td_{(H-L)}$	150	200	250	ns
Current sense clamp	V_{COMP} = Upper clamp, V_{MULT} = 1.5V	V_{CS}	0.97	1.02	1.07	V
Current sense offset	V_{MULT} = 0	Vcs_{offset}		25		mV
	V_{MULT} = 2.5V			5		
Zero current detector						
Upper clamp voltage	I_{ZCD} = 2.5mA	V_{ZCDH}	5.0	5.7	6.5	V
Lower clamp voltage	I_{ZCD} = - 2.5mA	V_{ZCDL}	-0.3	0	0.3	V
Arming voltage (positive-going edge)		V_{ZCDA}		1.4		V
Triggering voltage (negative-going edge)		V_{ZCDT}		0.7		V
Input bias current	V_{ZCD} = 1 to 4.5V	I_{ZCDb}		2		µA
Source current capability		I_{ZCDsrc}	-2.5			mA
Sink current capability		I_{ZCDsnk}	2.5			mA
Starter						
Start timer period		t_{START}	75	190	300	µs

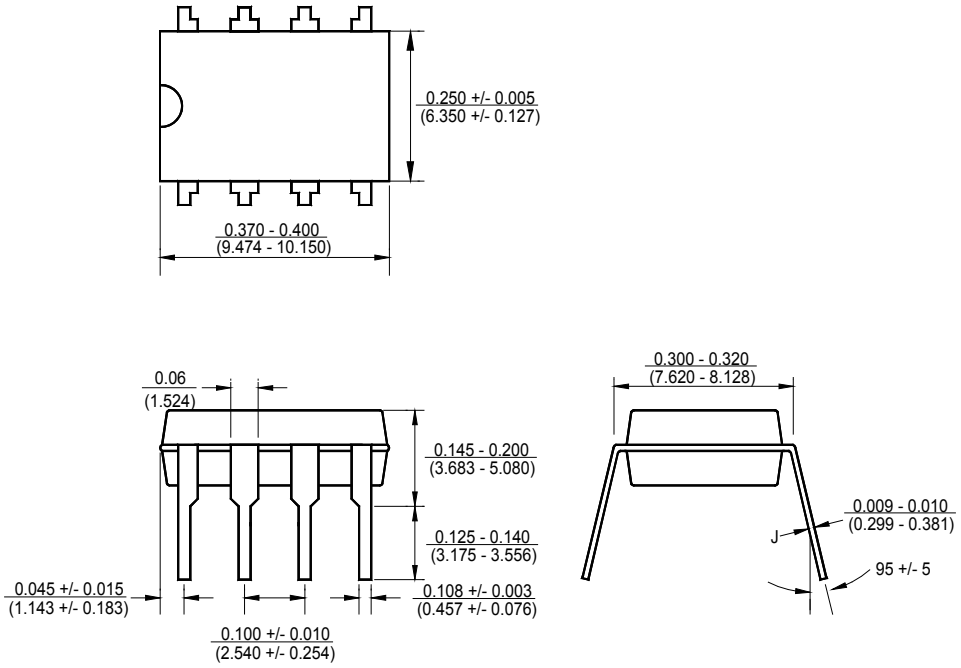
Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Gate driver						
Output low voltage	I_{sink} = 100mA	V_{OL}		0.6	1.2	V
Output high voltage	I_{source} = 5mA	V_{OH}	9.8	10.3		V
Peak source current		I_{srcpk}	-0.6			A
Peak sink current		I_{snkpk}	0.8			A
Voltage fall time		t_f		30	70	ns
Voltage rise time		t_r		60	110	ns
Output clamp voltage	I_{source} = 5mA; Vcc = 20 V	V_{Oclamp}	10	12	15	V
UVLO saturation	Vcc = 0 to V_{CCon}, I_{sink} = 2mA				1.1	V

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise specified

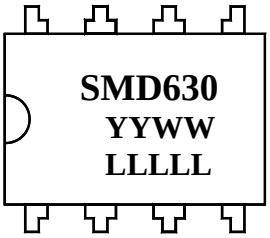
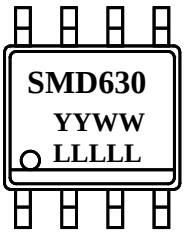
SO 8



DIP 8



MARKING DIAGRAM

DIP 8	SO 8
	

YY = Year, WW = Working Week, LLLLL = Lot number